FIG. 3

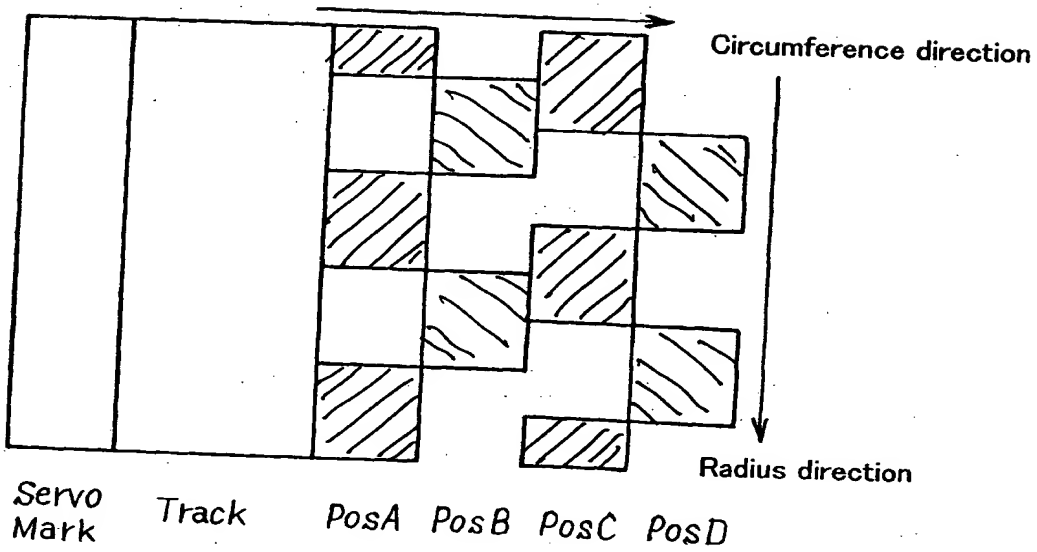


FIG. 4

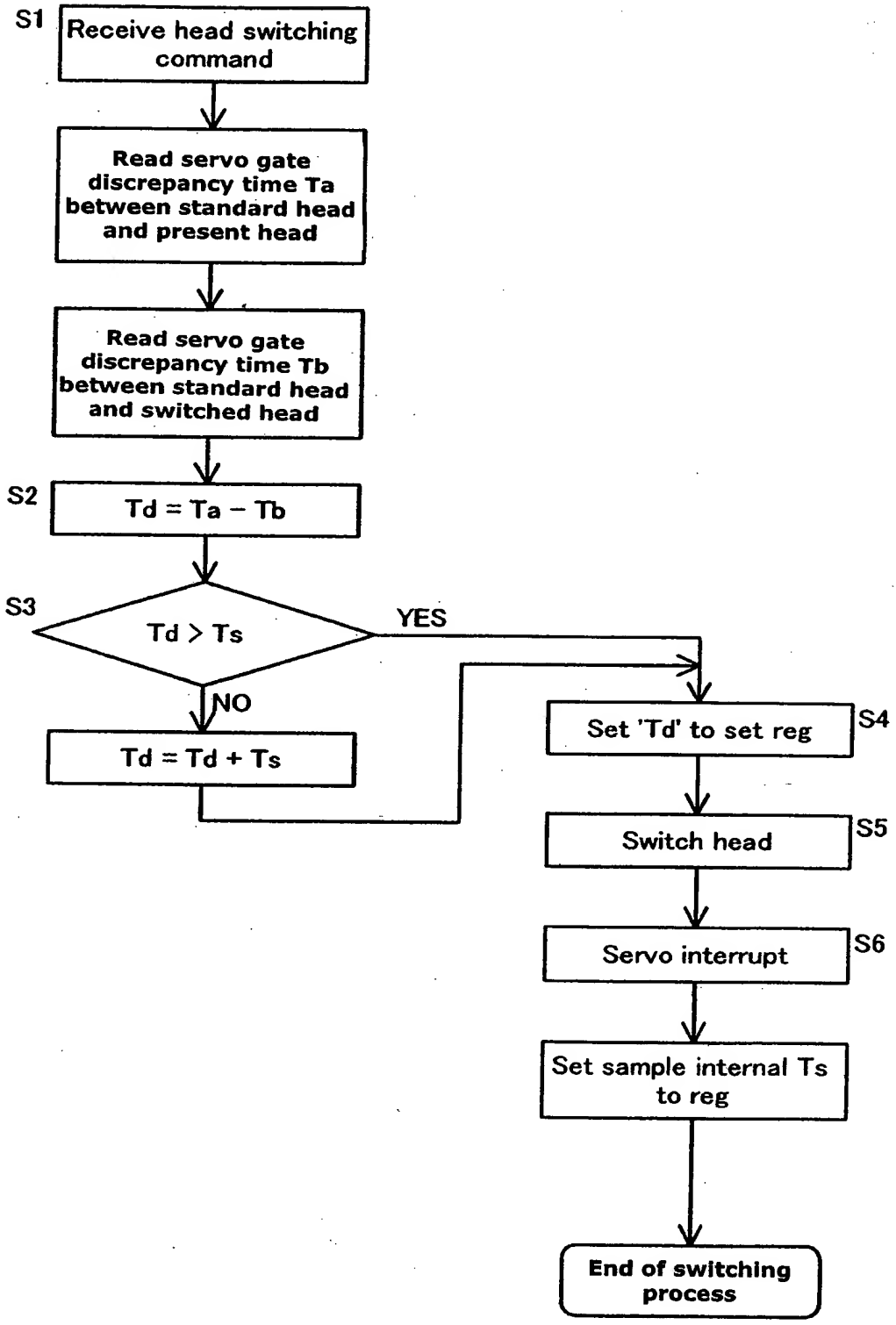

S1
Receive head switching command
Read servo gate discrepancy time Ta between standard head and present head
Read servo gate discrepancy time Tb between standard head and switched head
S2
Td = Ta – Tb
S3
Td > Ts
YES
NO
Td = Td + Ts
Set 'Td' to set reg
S4
Switch head
S5
Servo interrupt
S6
Set sample internal Ts to reg
End of switching process

FIG. 7

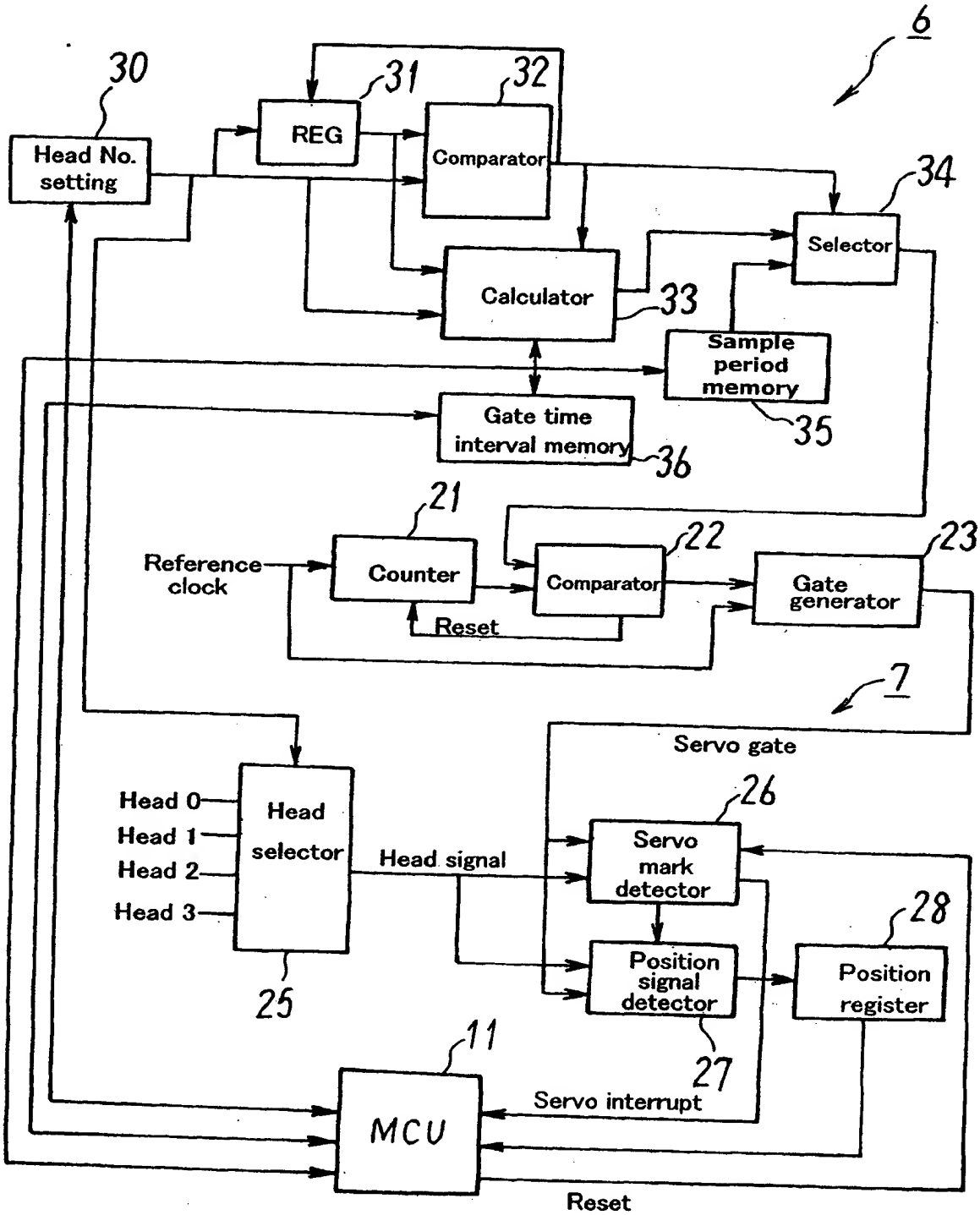

6
30
31
32
REG
Comparator
Head No. setting
34
Selector
Calculator
33
Sample period memory
35
Gate time interval memory
36
21
22
23
Reference clock
Counter
Comparator
Gate generator
Reset
7
Servo gate
26
Head 0
Head 1
Head 2
Head 3
Head selector
Head signal
Servo mark detector
28
Position signal detector
Position register
25
27
11
MCU
Servo interrupt
Reset

FIG. 8

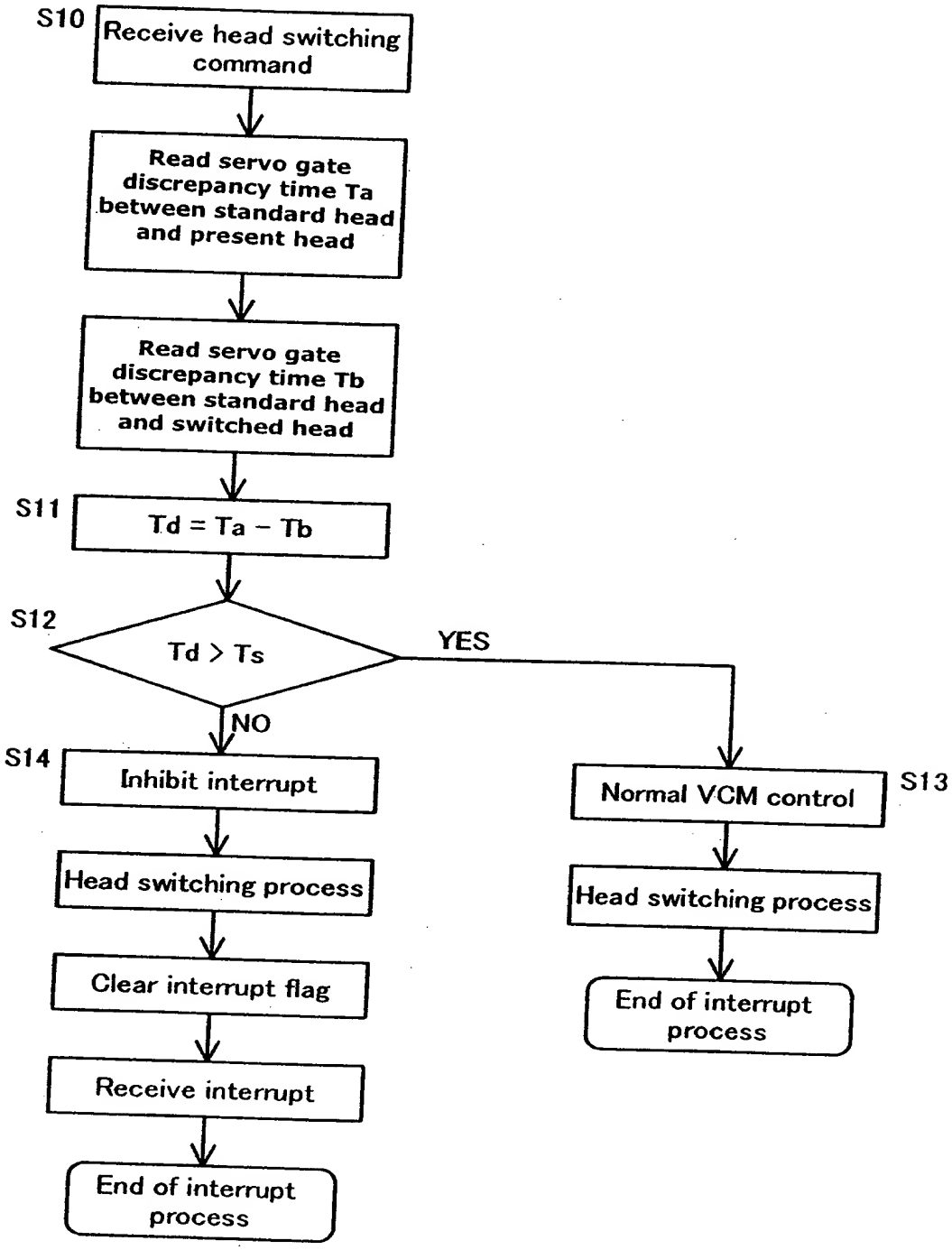
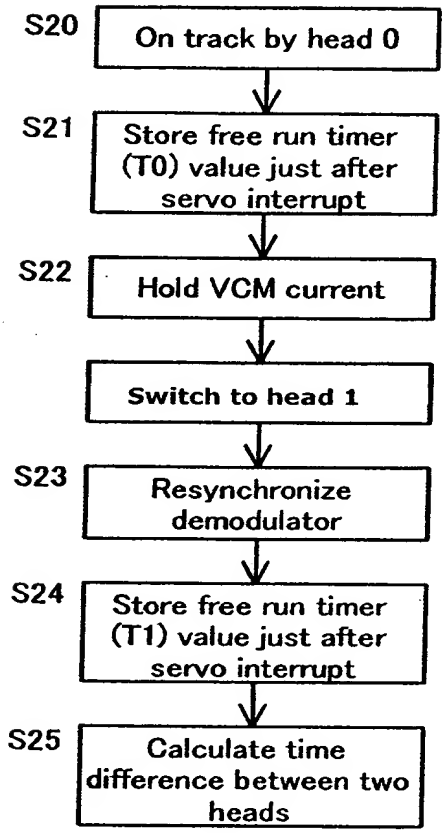

S10
Receive head switching command
Read servo gate discrepancy time Ta between standard head and present head
Read servo gate discrepancy time Tb between standard head and switched head
S11
Td = Ta – Tb
S12
Td > Ts
YES
NO
S14
Inhibit interrupt
Head switching process
Clear interrupt flag
Receive interrupt
End of interrupt process
Normal VCM control
S13
Head switching process
End of interrupt process

FIG. 10


S20
On track by head 0
S21
Store free run timer (T0) value just after servo interrupt
S22
Hold VCM current
Switch to head 1
S23
Resynchronize demodulator
S24
Store free run timer (T1) value just after servo interrupt
S25
Calculate time difference between two heads